

A 0.5-V Low-Power Negative Resistance-based TIA for Passive Down-conversion Mixer

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Abstract—This paper presents the design and simulation of a transimpedance amplifier (TIA) for the down-conversion of an RF mixer. The proposed TIA circuit is based on a negative resistance amplifier consisting of only a pair of resistors and a negative transconductor. It was developed in a 180-nm CMOS process, with a supply voltage of 0.5 V and a power dissipation of only 860 nW. The TIA has a gain of 201 kA/V, an input impedance of 18.7 k Ω , and a -3dB frequency of 2.5 MHz.

Index Terms—mixer, transimpedance, downconversion, negative resistance.

I. INTRODUCTION

Home automation along with the massive use of the Internet of Things (IoT) has increased the number of connected devices per person. A few years ago each person used to have only a personal computer and one smartphone connected to the internet, but nowadays is common to have some wearable and home devices also connected. It is estimated that by 2030 this number will reach 40 devices per person, generating an economic impact higher than 11 trillion a year [1].

Energy consumption is one of the main challenges of IoT devices. Thus, the power optimization and the design of novel circuit topologies are very important to design IoT circuits [2]. In IoT devices the highest power consumption used to be in the RF transceiver block, generally consuming more than 50% of the total power. This has enabled the development of new RF transceiver architecture, especially those operating with ultra-low supply voltage [3]–[5].

A typical RF receiver for low-voltage implementations is shown in Fig. 1. The front-end first active block is the low noise amplifier (LNA) that is used to amplify the received signal with low noise insertion. After the LNA, there is the frequency down-conversion stage performed by the mixer. Passive mixers and transimpedance amplifiers (TIA) are usually used for the down-conversion step. After the down-conversion process, the analog signal should be filtered, amplified and converted to the digital.

The down-conversion mixer is one of the main building blocks of an RF receiver since its noise figure and non-linearity are important to the performance specifications of modern RF circuit implementation. Recent proposals in the literature are increasing with the objective of improving the performance of passive mixers [6]–[8].

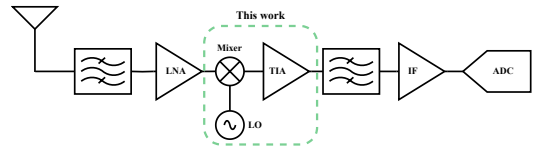


Fig. 1. Block diagram of a typical RF receiver, with Passive Mixer and transimpedance amplifier.

The TIA circuit used in RF receivers is generally implemented in CMOS process using classical operational amplifier topologies, such as multi-stage operational amplifiers and fully-differential amplifiers. However, these topologies present considerable power dissipation even at low-frequency operation [9]. Some novel amplifier topologies have been proposed in the literature by using active negative conductance circuits to compensate for the low voltage gain and reduced bandwidth of the amplifier without increasing the power consumption [11], [12]. In [3] and [10] a low voltage negative transconductance circuit is employed at the inputs of the single-stage fully differential amplifier to implement complex filters and variable gain amplifier to be used in low-energy RF receivers. Additionally, in [14] a simplified small-signal voltage amplifier based on using only resistors and negative resistance is introduced. This amplifier present reduced input impedance and high voltage gain, which are important characteristics for the implementation of a TIA. In this paper, we aim to present a preliminary analysis of using the negative resistance-based amplifier to implement the TIA of a passive down-conversion RF mixer. Schematic-level simulation results are presented for the circuit designed in a CMOS 180 nm process to operate with a 0.5 V power supply.

This paper is organized as follows: the analysis of the passive mixer with an ideal TIA is presented in Section II. In Section III the negative resistance-based TIA is analyzed and in Section IV the simulation results are presented. Finally, Section V presents the conclusions and proposes some future works.

II. PASSIVE MIXER WITH IDEAL AMPLIFIER

The TIA modeling can be performed using the quadrupole voltage amplifier model shown in Fig. 2. Its model is repre-

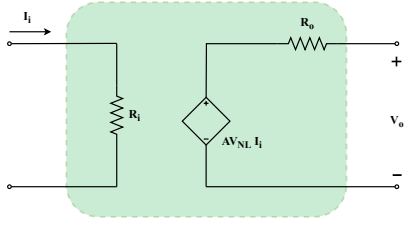


Fig. 2. Quadropole voltage amplifier model.

sented by the input resistance (R_i), output resistance (R_o), and of course, the non-load voltage gain (A_{vNL}).

When it is used as a TIA, the gain should be obtained through the ratio between the output voltage and the input current. From the amplifier circuit model given in Fig. 2, we observe that the input current (I_i) can be obtained by the ratio of V_i/R_i , thus the TIA gain can be obtained by (1). If a resistive load is considered, the TIA gain becomes equal to (2). This equation shows that when a load is added to the circuit the gain is reduced.

$$A_{v_{iNL}} = \frac{V_o}{I_i} = \frac{V_i \cdot A_{vNL}}{V_i/R_i} = R_i \cdot A_{vNL} \quad (1)$$

$$A_{v_i} = R_i \cdot A_{vNL} \cdot \frac{R_L}{R_L + R_o} \quad (2)$$

As we aim to operate with ultra-low voltage, 0.5 V in this paper, the TIA implementation should be based on fully differential amplifiers to improve the dynamic range. Fig. 3 shows the quadropole model of the fully differential TIA.

The basic structure of the mixer is shown in Fig. 4(a), where V_{LO} turns the switch on and off, producing $V_{IF} = V_{RF}$ or $V_{IF} = 0$. The circuit mixes the RF input with all the LO harmonics, resulting in “mixing spurs” which are the unwanted effects of its non-linearity. Figure 4 (b) shows the case where the passive mixer is powered by a current source. In this case, it is considered that the LNA has a relatively high output impedance, approaching a current source. Incoming current flows to the top node about half of the time and flows through Z_{BB} . In the time domain, it can be represented as (3), $S(t)$ represents a square wave that alternates between 0 and 1, and $h(t)$ is the Z_{BB} impulse response. The expression 4 in the frequency domain, represents $S(f)$ as the spectrum of a square wave. After convolution with the first harmonic

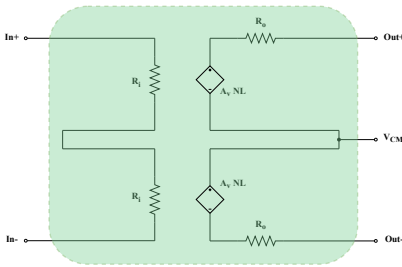


Fig. 3. Quadropole voltage amplifier model of the fully-differential TIA.

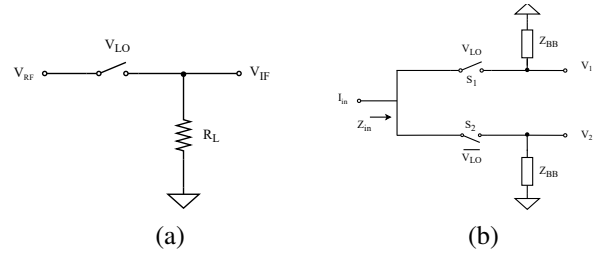


Fig. 4. Basic structure of an ideal mixer powered by a voltage source (a) and a current source (b).

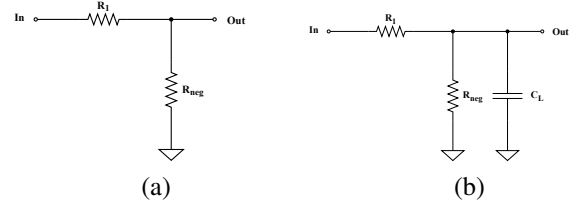


Fig. 5. Basic circuit for negative resistance based-amplifier analysis. (a) low-frequency representation and (b) single-pole circuit.

of $S(f)$, $I_{in}(f)$ is transposed to the baseband and is then subjected to the frequency response of $Z_{BB}(f)$. A similar phenomenon happens at the bottom node, but as s_2 is driven by $\overline{V_{LO}}$ it presents 180° phase difference, generating a differential signal output.

$$V_1(t) = [i_{in}(t) \times S(t)] * h(t) \quad (3)$$

$$V_1(f) = [I_{in}(f) * S(f)] \cdot Z_{BB}(f) \quad (4)$$

Designing the circuit to operate at low voltages helps maintain linearity. Unlike the RF port, the mixer is considered non-linear with respect to the LO port. Ideally, the output amplitude and phase at the IF port is dependent on the amplitude and phase of the signal at the RF port and independent of the same at the LO port. However, depending on the port-to-port isolation, the output dependency on the LO signal characteristics varies. Isolation between ports is important as the presence of a feedthrough signal on another port can affect the linearity and noise figure of the mixer.

III. NEGATIVE RESISTANCE-BASED TIA

The negative resistance-based fundamental amplifier is modeled using a voltage divider, shown in Fig. 5 (a). In which R_{neg} is an active resistor. The voltage gain (A_v) can be modeled as (5). If only positive resistors are used, its behavior will be that of a voltage attenuator. However, if R_{neg} is negative, the $R_1 + R_{neg} \ll R_{neg}$ causing the circuit to behave as a voltage amplifier. It presents the capability of to operate as an inverting or non-inverting amplifier, depending on the denominator of (5). If $R_{neg} < -R_1$ the circuit works as an inverter amplifiers, and if $R_{neg} > -R_1$ is equivalent to a non-inverter amplifier [14].

$$A_v = \frac{V_{out}}{V_{in}} = \frac{R_{neg}}{R_1 + R_{neg}} \quad (5)$$

As shown in the circuit in Fig. 5(a), the input impedance is also affected by the negative resistance. It goes to zero when R_{neg} tends to $-R_1$, as shown in (6).

$$Z_{in} = R_1 + R_{neg} \quad (6)$$

Based on (5) and (6), it is possible to obtain the voltage to current gain of the amplifier working as TIA, as given by (7). It is important that the TIA gain depends only of R_{neg} .

$$A_{vi} = \frac{V_{out}}{I_{in}} = \frac{R_{neg}}{R_1 + R_{neg}} \cdot (R_1 + R_{neg}) = R_{neg} \quad (7)$$

The analysis of the frequency response involves examining the parallel combination of a load C_L and R_{neg} , as depicted in Fig. 5(b). This load also represents the parasitic capacitances present due to the implementation of the negative resistance. The voltage gain, considering C_L can be evaluated by (8). In the same way, the input impedance is also dependent on C_L as given by (9).

$$A_V(s) = \frac{R_{neg}}{s \cdot R_1 \cdot R_{neg} \cdot C_L + R_1 + R_{neg}} \quad (8)$$

$$Z_{in} = R_1 + \frac{R_{neg}}{s \cdot R_{neg} \cdot C_L + 1} \quad (9)$$

With the previous analysis, we can conclude that is possible to implement a TIA using a negative resistance amplifier since it has a low input impedance and can have high gain.

In this project, the negative resistance is implemented using the cross-coupled negative transconductor. Its schematic is shown in figure 6. This topology is composed of two PMOS transistors (M_1 and M_2), with equal W/L ratio, functioning as cross-coupled transconductors and two NMOS transistors (M_3 and M_4) working as current source loads [5]. The transistor M_5 works as an active diode in order to mirror the I_{ref} current to the M_3 and M_4 transistors.

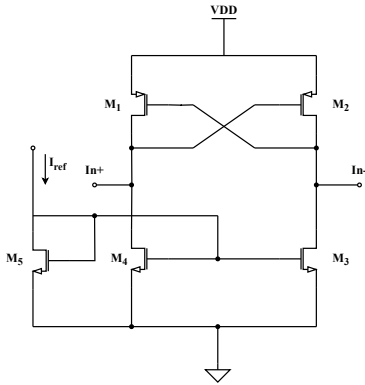


Fig. 6. Negative transconductor with Cross-Coupled and current mirror.

The small-signal model of this circuit gives us symmetrical input voltages because it is a differential circuit. Equations (10) and (11) are obtained by the low-frequency small-signal circuit analysis considering the common-mode signals at nodes $In+$ and $In-$ in both the circuit branches.

In these equations g_{m1} and g_{m2} represent the transconductances of M_1 and M_2 , g_{ds1} and g_{ds2} the output conductance of M_1 and M_2 and g_{ds3} and g_{ds4} the output conductance of M_3 and M_4 .

$$g_{m1} \cdot v_{in-} + g_{ds4} \cdot v_{in+} + g_{ds1} \cdot v_{in+} = i_{in+} \quad (10)$$

$$g_{m2} \cdot v_{in+} + g_{ds3} \cdot v_{in-} + g_{ds2} \cdot v_{in-} = i_{in-} \quad (11)$$

Considering the $g_{m1} = g_{m2} = g_{mP}$, $g_{ds1} = g_{ds2} = g_{dsP}$, $g_{ds3} = g_{ds4} = g_{dsN}$ and $v_{in+} = -v_{in-}$, the small signal equivalent negative resistance (R_{neg}) at the circuit can be obtained as shown in (12).

$$R_{neg} = -\frac{1}{g_{mP} + g_{dsP} + g_{dsN}} \approx -\frac{1}{g_{mP}} \quad (12)$$

The value of R_{neg} can be adjusted according to the DC voltage level, the transistor sizes, and the I_{ref} current level. The value of the negative resistance is also inversely dependent on the PMOS transconductance g_{mP} . Therefore, the g_m/I_D ratio shows that the negative resistance depends on the mirror current I_{ref} . The design should be performed to obtain the target TIA gain and the value of $|R_{neg}|$ should be near R_1 in order to obtain a reduced input impedance value.

IV. SIMULATED RESULTS

The negative resistance-based TIA was implemented in a 180 nm CMOS technology using low-VT transistors to operate with a supply voltage of 0.5 V. Because of this, the transistors are operating at moderate inversion. The transistors of the circuit from Figure 6 were sized according to [13] in order to obtain a negative resistance in the range of -100 k Ω . The value of R_1 was defined to be equal to 110 k Ω to make the input impedance to be around 10 k Ω (or 20 k Ω in differential mode). The TIA gain, as shown in (7) is equal to R_{neg} , thus 100 kV/A (or 200 kV/A in differential mode) in this implementation.

The complete circuit presents a power dissipation of 0.86 μ W at 0.5 V of V_{DD} . Figure 7 shows the TIA gain as a function of the frequency. The low-frequency differential-mode gain is 106.1 dB or 201.8 kV/A and the -3dB frequency is approximately 2.5 MHz, considering a capacitive load (C_L) of 100 fF. The simulated differential-mode input impedance of the TIA as a function of the frequency is shown in Fig. 8. It presents a value of 18.71 k Ω at low frequency and its value is around 50 k Ω at 2.5 MHz. Figures 9 and 10 show the results of the Monte Carlo analysis with 200 simulations for the gain and input impedance of the circuit. These graphs show that the circuit is sensitive for process variation, that can be improved by using a robust biasing circuit or employing calibration after the fabrication.

V. CONCLUSION

This paper has presented the design of a low-power and low-voltage transimpedance amplifier that aims to be used in passive mixer implementation. The TIA proposed is based on using a negative resistance amplifier that is composed only

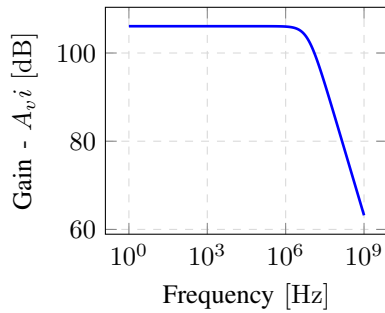


Fig. 7. TIA gain as a function of the frequency.

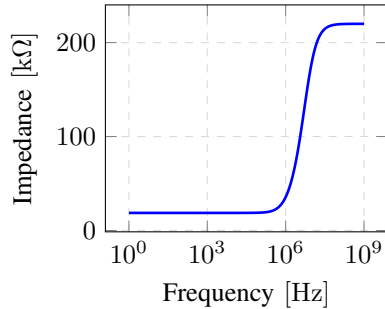


Fig. 8. TIA input impedance as a function of the frequency.

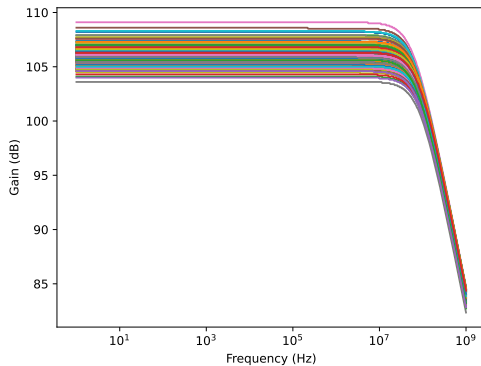


Fig. 9. Frequency response for the circuit gain, obtained through 200-runs Monte Carlo analysis.

of a pair of resistors and a negative transconductor circuit. The implemented circuit in a CMOS 180 nm technology presented power dissipation of only 860 nW, input impedance of 18.71 k Ω , a gain of 106 dB, and -3 dB frequency of 2.5 MHz. In future works we intend to design a passive mixer using the proposed TIA and to prototype the circuit for experimental validation.

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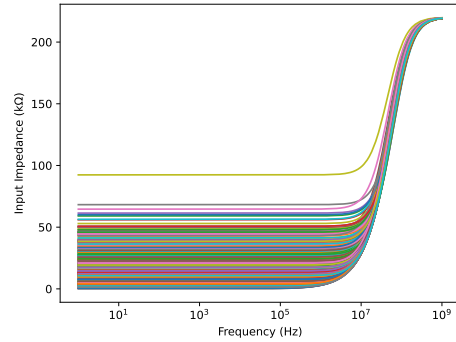


Fig. 10. Input impedance obtained with 200-runs Monte Carlo analysis.

REFERENCES

- [1] Manyika, James. The Internet of things, available on: <https://www.mckinsey.com/mgi/overview/in-the-news/by-2025-internet-of-things-applications-could-have-11-trillion-impact>, 2015.
- [2] E. Kargaran, D. Manstretta and R. Castello, "Design Considerations for a Sub-mW Receiver Front-End for Internet-of-Things," in *IEEE Open Journal of the Solid-State Circuits Society*, vol. 1, pp. 37-52, 2021.
- [3] M. Ding et al., "A 0.8V 0.8mm² bluetooth 5/BLE digital-intensive transceiver with a 2.3mW phase-tracking RX utilizing a hybrid loop filter for interference resilience in 40nm CMOS," 2018 *IEEE International Solid - State Circuits Conference - (ISSCC)*, San Francisco, CA, USA, 2018, pp. 446-448, doi: 10.1109/ISSCC.2018.8310376.
- [4] Kuo, Feng-Wei, Sandro Binsfeld Ferreira, Ron Chen, Lan-Chou Cho, Chewn-Pu Jou, Mark Chen, Masoud Babaie, and Robert Bogdan Staszewski. "Towards Ultra-Low-Voltage and Ultra-Low-Power Discrete-Time Receivers for Internet-of-Things." 2018 *IEEE/MTT-S International Microwave Symposium - IMS (2018)*: 1211-214.
- [5] Yi, Haidong, Wei-Han Yu, Pui-In Mak, Jun Yin, and Rui P. Martins. "A 0.18-V 382- μ W Bluetooth Low-Energy Receiver Front-End With 1.33-nW Sleep Power for Energy-Harvesting Applications in 28-nm CMOS." *IEEE Journal of Solid-state Circuits* 53.6 (2018): 1618-627.
- [6] K. Balaban, M. M \ddot{o} ck and A. \mathcal{C} . Ulusoy, "A Highly Linear D-Band Broadband Down Conversion Mixer in 22-nm FDSOI CMOS," 2023 *IEEE 23rd Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems*, Las Vegas, NV, USA, 2023, pp. 1-3, doi: 10.1109/SiRF56960.2023.10046276.
- [7] S. Weinreich and B. Murmann, "A 0.6–1.8-mW 3.4-dB NF Mixer-First Receiver With an N-Path Harmonic-Rejection Transformer-Mixer," in *IEEE Journal of Solid-State Circuits*, vol. 58, no. 6, pp. 1508-1518, June 2023, doi: 10.1109/JSSC.2022.3214226.
- [8] H. Shao, P. -I. Mak, G. Qi and R. P. Martins, "A 266-W Bluetooth Low-Energy (BLE) Receiver Featuring an N-Path Passive Balun-LNA and a Pipeline Down-Mixing BB-Extraction Scheme Achieving 77-dB SFDR and 3-dBm OOB-B1 dB," in *IEEE Journal of Solid-State Circuits*, vol. 57, no. 12, pp. 3669-3680, Dec. 2022, doi: 10.1109/JSSC.2022.3200932.
- [9] Kim, Namsoo, Vladimir Aparin, and Lawrence E Larson. "A Resistively Degenerated Wideband Passive Mixer With Low Noise Figure and High." *IEEE Transactions on Microwave Theory and Techniques* 58.4 (2010): 820-30.
- [10] Severo, L. Compassi, Van Noije, W, A 0.4-V 10.9- W/Pole Third-Order Complex BPF for Low Energy RF Receivers, *IEEE Transactions on Circuits and Systems I: Regular Papers*, 66 (6), 2, 2019.
- [11] Ananda Mohan, P. (2020), Analysis of negative-R assisted integrators and differentiators. *Electron. Lett.*, 56: 123-125, 2020.
- [12] Razavi, Behzad, *RF Microelectronics*, Nova York, Prentice Hall, 2012.
- [13] Girardi, A. G., Compassi-Severo, L, de Aguirre, P. C. C., Design Techniques for Ultra-Low Voltage Analog Circuits Using CMOS Characteristic Curves: a practical tutorial, *Journal of Integrated Circuits and Systems*, vol. 17, n.1, 2022.
- [14] S. Santos, M. Mikue, L. Compassi-Severo, "A Low-Power 0.4-V Negative Resistance-Based Small-Signal Amplifier", 22nd *Microelectronics Students Forum (SFORUM)*, virtual, 2022.